REMARKS

In view of the remarks below, the Applicants respectfully assert that the objections and rejections to the pending claims are now moot, and that the pending claims are in condition for allowance.

Claim Rejections – 35 U.S.C. §112 & Objections to Specification

In the Office Action, Claims 1-22 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Moreover, the Examiner objected to the specification for failing to provide proper antecedent basis for the claimed subject matter. For both the rejection and objection, the Office Action states that while Claims 1, 8 and 15 all recite, "wherein at least two interconnections interconnect each processing element to at least two other processing elements", FIGS. 1A-1C of the specification depict each processing element connected to only one other processing element, and there is no facility for two interconnections. With regard to the rejection under 35 U.S.C. § 112 and objection to the specification, Applicants respectfully assert that FIGS. 1A-1C, as currently presented, each show processing elements where at least two interconnections interconnect each processing element to at least two other processing elements.

FIGS. 1A-1C of the specification show processing elements (PEs), represented by shaded circles, connected to their respective adjacent PEs through straight-line interconnections. The straight-line interconnections provide at least one connection for a PE to an adjacent PE. Moreover, for a PE located between two other PEs, the straight-line

interconnections provide two interconnections to two other PEs. FIGS. 1A-1C also show arcing lines which represent a second (or perhaps third) interconnection connecting one PE to a remote PE, which is a different PE than those PEs connected to it through the straight-line interconnection(s).

The narrative of page 9, lines 15-18, of the specification references FIGS. 1A-1C and confirms that they illustrate the interconnecting of two or more processing elements using at least two interconnections:

> "Referring to FIGS. 1A-1C, one-dimensional PDES can be implemented in a scalable computer architecture 10 by interconnecting each PE 12 to two or more PEs, with at least one PE further interconnected to at least one additional PE located remote from the respective at least one PE."

In addition, page 10 lines 5-8, describes how such connections are shown in those figures:

> "As illustrated with respect to three connections between PEs, consider the PEs connected on a line, with each PE 12 connected to each nearest-neighbor PE. Additionally, each PE is connected to at least one additional, remote PE (one as illustrated). It should be understood that although the PEs on each end of the line illustrated have no outermost neighbor, the outermost PE would typically be connected to each other as their respective outermost neighbor connection."

Therefore, FIGS 1A-1C and the narrative of the specification show an exemplary configuration of PEs and their interconnections that demonstrates, teaches and enables, "at least two interconnections interconnect each processing element to at least two other processing elements" which is recited in independent Claims 1, 8 and 15. Therefore, Applicants respectfully submit that the claims fully satisfy the requirements of 35 U.S.C. § 112, and thus, are in condition for allowance.

Claim Rejections – 35 U.S.C. §102 and §103

Claims 1, 8, and 15 are rejected under 35 U.S.C. §102(b) as being anticipated by *Nickolls* (5,598,408). For this rejection, the Office Action states that "*Nickolls* discloses a scalable processor including a plurality of processing elements PE1 to PE16 in figure 4A-1, which where target stage latches 445a-455f and 415a-415p provide interconnections which enable two interconnections to connect each processing element to at least two other processing elements." Applicants respectfully assert that *Nickolls* does not teach, suggest, or motivate "at least two interconnections interconnect each processing element to at least two other processing elements" which is recited in independent Claims 1, 8 and 15. Further, Applicant respectfully asserts that *Nickolls* does not teach, suggest, or motivate "the number of interconnections between processing elements is independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of interconnections between processing elements, thereby permitting connectivity between the processing elements to be scalable."

With regard to the rejection under U.S.C. § 102(b), while *Nickolls* discloses parallel processing arrays, the disclosed architecture of *Nickolls* does not teach or suggest the processing architecture of Applicants' claims. As shown in Figure 4A-1 of *Nickolls*, each processing element must go through a dedicated latch or switch to connect to another processing element on the same board or connect to an I/O interface to communicate with another board (*see Nickolls*, Figures 4A-1, col. 17, lines 26-67). To send data between processing elements, the *Nickolls* architecture partitions a message routing path and provides registers (i.e., latches) at the partition junctions to temporarily store bits of a transmitted message. When the bits of a serially

transmitted message are pipelined in a spatially distributed manner along a single message routing path serial bits can propogate simultaneously through short segments of the message routing path and connect one processing element with any other specified processing element on the board. *See Nickolls* Col 6. line 10- 33. *Nickolls* specifically states: "After a routing path is formed ("opened"), messaging can take place from the route originating processor PEx to the target processor PEy . . ." *Nickolls*, Col 17 lines 63-67. Thus, the connection of processing elements is always over a single message routing path. Therefore, the routing paths of *Nickolls* provide only a one-to-one connection path between PEs, and control bits (or signals) switch the connection path to create a new one-to-one connection between PEs. Moreover, the connection must be facilitated through the use of one or more intermediaries such as latches or switches. Therefore, *Nickolls* does not teach, suggest, or motivate the use of "at least two interconnections interconnect[ing] each processing element to at least two other processing elements" as required by independent Claims 1, 8 and 15.

Additionally, the PEs in *Nickolls* are arranged in a regular array with regular connections. In these regular array arrangements the number of interconnections (or possible interconnecting paths as in *Nickolls*) is dependent on the number of PEs in the regular array. As a result, regular arrays are limited in there ability to handle scalable simulations. In other words, in a regular array configuration, as the number of PEs increase, either the number of connection paths would have to increase or the size of each PE (i.e., the memory size, cache size, and processor speed) would have to increase to keep the same algorithmic efficiency.

In contrast to the configuration of a regular array, Independent Claim 1, 8 and 15 recite the limitation of:

> wherein the number of interconnections between processing elements is independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of interconnections between processing elements, thereby permitting connectivity between the processing elements to be scalable.

Unlike the regular array configuration disclosed in *Nickolls*, providing this scalability by allowing the number of interconnections between PEs to be independent of the number of PEs can keep the algorithmic efficiency constant without the need to increase either the memory size, cache size, or processor speed of each PEs or the number of connections to a single PE. This is achieved by adding random connections to any regular array of connected PEs. These small world random connections allow for a scalable computer arrangement. Therefore, *Nickolls* does not teach, suggest, or motivate having "the number of interconnections between processing elements [being] independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of interconnections between processing elements, thereby permitting connectivity between the processing elements to be scalable" as required by independent Claims 1, 8 and 15.

In the Office Action, Claims 2-7, 9-14, and 16-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Nickolls* (5,598,408) in view of Applicants' statements. For the reasons stated above, Applicants respectfully assert that *Nickolls* does not teach, suggest, or motivate what is described in Claims 1, 8, and 15. Therefore, dependent claims 2-7, 9-14, and 16-22 are allowable as a matter of law, and Examiner's contentions under §103(a) are now moot.

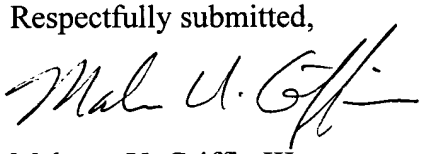
Conclusion

The foregoing is submitted as a full and complete response to the first Office Action. Applicants request that all pending claims be allowed because, as shown above, they are

patentable over the art of record. It is therefore respectfully requested that a Notice of Allowance be issued. If there are any issues that can be resolved by a telephone conference or an Examiner's Amendment, the Examiner is invited to call the undersigned attorney at (404) 853-8233.

I t is not believed that extensions of time or fees for addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 19-5029.

Respectfully submitted,



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I hereby certify that this paper, along with any paper referred to as being attached or enclosed, is being deposited with the United States Postal Service on May 3, 2005 with sufficient postage as first-class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Rebecca L. Smith